In the Claims:

Claims 1-27 are pending in this application, and the status of each is listed below.

1. (currently amended) An imaging system comprising:

an image capture circuit;

image processing circuitry, coupled to the image capture circuit, that is operable at a first rate and a second rate;

the image processing circuitry operating at the first rate to perform a first stage of image processing;

an intermediate storage queue, communicatively coupled to the image processing circuitry, that stores representations of a plurality of images having undergone the first stage of image processing in anticipation of the second stage of image processing;

the image processing circuit operating at the second rate to perform a second stage of image processing; and

at least one of the first rate and the second rate being adjustable.

2. (canceled)

3. (currently amended) The imaging system of claim [[2]] 1 wherein the second rate is adjusted based on the content of the intermediate storage queue.

4. (currently amended) The imaging system of claim [[2]] 1 wherein the first rate is adjusted based on the content of the intermediate storage queue.

5. (currently amended) The imaging system of claim [[2]] 1 wherein the second rate is adjusted down when the intermediate storage queue contains less than a predetermined amount of image data.

6. (currently amended) The imaging system of claim [[2]] 1 wherein the first rate is adjusted to zero when the intermediate storage queue is at least almost full.

7. (currently amended) The imaging system of claim [[2]] 1 wherein the second rate is adjusted to a maximum rate when the intermediate storage queue is at least almost full.

8. (currently amended) The imaging system of claim [[2]] 1 wherein the first rate is adjusted to a low rate when the intermediate storage queue contains more than a predetermined amount of image data.

9. (currently amended) The imaging system of claim [[2]] 1 wherein the second rate is adjusted to a high rate when the intermediate storage queue contains more than a predetermined amount of image data.

10. (original) An electronic imager, the electronic imager performing processing on an acquired image, the electronic imager comprising:

a plurality of functional processing circuits, the functional processing circuits comprising:

an acquisition circuit that produces signals in response to incident light from an acquired image;

an interface circuit, communicatively coupled to the acquisition circuit, that produces a raw image data set from the signals collected by the acquisition circuit;

a processing circuit that produces a processed image data set from the raw image set; and

an intermediate image storage buffer, communicatively coupled to the processing circuit, that stores one or more image data sets; and

one or more of the plurality of functional processing circuits altering its particular operational speed in response to the amount of image data sets contained in the intermediate storage buffer.

11. (original) The electronic imager of claim 10, wherein the intermediate storage buffer stores raw image data sets.

12. (original) The electronic imager of claim 11 wherein the processing circuit slows when the amount of raw image data sets exceeds a predetermined threshold.

13. (original) The electronic imager of claim 11 wherein the processing circuit speeds up when the amount of raw image data sets is below a predetermined threshold.

14. (original) The electronic imager of claim 11 wherein the acquisition circuit slows when the amount of raw image data sets exceeds a predetermined threshold.

15. (original) The electronic imager of claim 10, the functional processing circuits further comprising a transformation circuitry, communicatively coupled to the processing circuitry, that produces a final data image set from a processed data image set.

16. (original) The electronic imager of claim 15 wherein the intermediate storage buffer stores processed image data sets.

17. (original) The electronic imager of claim 16 wherein the processing circuit slows when the amount of processed image data sets exceeds a predetermined threshold.

18. (original) The electronic imager of claim 16 wherein the processing circuit speeds up when the amount of processed image data sets is below a predetermined threshold.

19. (original) A method of operating an imaging system, the imaging system comprising functional imaging circuits, the functional image circuits comprising an image sensor, an interface circuit, and an image processing circuit, the method comprising the steps of:

acquiring an initial image from the image sensor;

producing a first image data from the initial image in the interface circuit;

processing the first image data into a second image data in the image

processing circuit;

selectively storing either the first image data or the second image data in a buffer; and

selectively altering the speed at which one of the functional imaging circuits operates in response to the amount of image data in the buffer.

20. (original) The method of claim 19, the functional imaging circuits further comprising a transformation circuit, the method further comprising the step of: processing the second image data into a final image data in the transformation circuit.

21. (original) The method of claim 20 wherein the step of selectively altering further comprises the step of speeding up the transformation circuit when the buffer contains more than a predetermined amount of processed image data.

22. (original) The method of claim 20 wherein the step of selectively altering further comprises the step of slowing down the transformation circuit when the buffer contains less than a predetermined amount of processed image data.

23. (original) The method of claim 20 wherein the step of selectively altering further comprises the step of slowing down the processing circuit when the buffer contains more than a predetermined amount of processed image data.

24. (original) The method of claim 19 wherein the step of selectively altering further comprises the step of slowing down the processing circuit when the buffer contains less than a predetermined amount of raw image data.

25. (original) The method of claim 19 wherein the step of selectively altering further comprises the step of speeding up the processing circuit when the buffer contains more than a predetermined amount of raw image data.

26. (original) The method of claim 19 wherein the step of selectively altering further comprises the step of slowing down the interface circuit when the buffer contains more

than a predetermined amount of raw image data.

27. (original) The method of claim 19 wherein the step of selectively altering further comprises the step of slowing down the image sensor when the buffer contains more than a predetermined amount of raw image data.